CLAIMS

1. A circuit comprising

a spin transistor having transfer characteristics depending on the spin direction of conduction carriers,

the spin direction of the conduction carriers being changed so as to vary the transfer characteristics of the spin transistor,

an operating point being changed based on the transfer characteristics, thereby reconfiguring a function.

2. A circuit comprising

a spin transistor that includes at least two ferromagnetic layers, and has transfer characteristics depending on the magnetization state of the ferromagnetic layers,

the magnetization state of the spin transistor being changed to move an operating point, thereby reconfiguring a function.

3. The circuit as claimed in claim 2, wherein:

the spin transistor has at least one ferromagnetic body ("free layer") with a magnetization direction that can be controlled independently, and at least one ferromagnetic body ("pin layer") with a fixed magnetization direction; and

the circuit reconfigures a function by changing an operating point based on two magnetization states including a first state in which the free layer and the pin layer have the same magnetization directions ("parallel magnetization"), and a second state in which the free layer and the pin layer have the opposite magnetizing states to each other ("antiparallel magnetization").

4. The circuit as claimed in any of claims 1

to 3, further comprising:

a first terminal that generates the operating point and serves as an output;

a first circuit group for charging the first terminal; and

a second circuit group for discharging the first terminal,

wherein the spin transistor is included in one or both of the first circuit group and the second circuit group.

5. The circuit as claimed in claim 4, wherein the first terminal has a potential that is determined by changing the spin directions of the carriers of the spin transistor or by controlling the transfer characteristics depending on the magnetization state of the spin transistor.

6. The circuit as claimed in any of claims 1 to 5, which outputs a signal based on a signal that is input via a neuron MOS (νMOS) structure including a plurality of inputs weighted with capacitances by capacitors and a floating gate connecting the inputs.

7. The circuit as claimed in claim 6, wherein the input signals are weighted so as to be substantially equal to one another.

8. The circuit as claimed in any of claims 4 to 7, wherein a logic threshold value for dividing the potential generated in the first terminal into an output of a logic level "0" and an output of a logic level "1" is set with respect to the operating point that varies according to a variation in the transfer characteristics of the spin transistor.

9. The circuit as claimed in any of claims 1

to 8, wherein an A-D converter with a predetermined logic threshold value is connected to an output terminal of the circuit.

10. The circuit as claimed in any of claims 1 to 9, wherein the spin transistor is a MOSFET-type spin transistor ("spin MOSFET") that are formed with a source and a drain, including a MOS structure and a ferromagnetic body.

11. The circuit as claimed in any of claims 3 to 9, wherein the first circuit group includes a MOSFET of a first conductivity type or a spin MOSFET of the first conductivity type, and the second circuit group includes a MOSFET of the same conductivity type as the first conductivity type or a spin MOSFET of the same conductivity type as the first conductivity type.

12. The circuit as claimed in any of claims 3 to 11, comprising

an E/E circuit that includes a structure in which the source of an enhancement MOSFET or an enhancement spin MOSFET contained in the first circuit group is connected to the drain of an enhancement MOSFET or an enhancement spin MOSFET contained in the second circuit group, and a first terminal that is formed at the connection portion.

13. The circuit as claimed in claim 12, wherein the drain of an enhancement MOSFET or an enhancement spin MOSFET contained in the first circuit group in the E/E circuit is connected to the gate of the enhancement MOSFET or the enhancement spin MOSFET.

14. The circuit as claimed in claim 12 or 13, wherein an enhancement MOSFET or an enhancement spin MOSFET contained in the second circuit group in the E/E

circuit has a νMOS structure.

15. The circuit as claimed in any of claims 3 to 11, comprising

an E/D circuit that includes a structure in which the source of a depletion MOSFET or a depletion spin MOSFET contained in the first circuit group is connected to the drain of an enhancement MOSFET or an enhancement spin MOSFET contained in the second circuit group, and a first terminal that is formed at the connection portion.

16. The circuit as claimed in claim 15, wherein the source of a depletion MOSFET or a depletion spin MOSFET contained in the first circuit group in the E/D circuit is connected to the gate of the depletion MOSFET or the depletion spin MOSFET.

17. The circuit as claimed in claim 15 or 16, wherein an enhancement MOSFET or an enhancement spin MOSFET contained in the second circuit group in the E/D circuit has a νMOS structure.

18. The circuit as claimed in any of claims 11 to 17, wherein the νMOS structure has two inputs (A and B) weighted with capacitances by capacitors.

19. The circuit as claimed in any of claims 4 to 18, wherein the circuit is a NAND/NOR reconfigurable logic circuit or an AND/OR reconfigurable logic circuit that includes the A-D converter having the first terminal as an input.

20. The circuit as claimed in any of claims 11 to 19, wherein the first and second circuit groups or one of the first and second circuit groups comprises a circuit that controls the potential of the

first terminal by connecting the source or the drain of another spin MOSFET to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET, the level shift circuit turning on the another spin MOSFET only when a predetermined input is made.

21. The circuit as claimed in any of claims 11 to 20, wherein the second circuit group comprises

a circuit that controls the potential of the first terminal by connecting the drain of another spin MOSFET of n-channel type to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET of n-channel type, the another spin MOSFET of n-channel having the source grounded, the level shift circuit turning on the another spin MOSFET of n-channel type only when an input is A = B = "0".

22. The circuit as claimed in any of claims 11 to 21, wherein the first circuit group comprises

a circuit that controls the potential of the first terminal by connecting the drain of another spin MOSFET of p-channel type to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET of p-channel type, the another spin MOSFET of p-channel having the source connected to a supply voltage, the level shift circuit turning on the another spin MOSFET of p-channel type only when an input is A = B = "1".

23. The circuit as claimed in any of claims 20 to 23, wherein the level shift circuit is formed with an E/E, E/D, or CMOS inverter.

24. The circuit as claimed in any of claims 20 to 23, wherein the circuit is a reconfigurable logic circuit that includes the A-D converter having the

first terminal as an input.

25. The circuit as claimed in claim 20 or 24, wherein the circuit is a reconfigurable logic circuit that includes an inverter having the output of the A-D converter as an input, and can achieve all symmetric Boolean functions.

26. The circuit as claimed in any of claims 3 to 9, wherein the first circuit group includes a MOSFET of a first conductivity type or a spin MOSFET of the first conductivity type, and the second circuit group includes a MOSFET of a second conductivity type different from the first conductivity type or a spin MOSFET of the second conductivity type.

27. The circuit as claimed in claim 26, comprising

a CMOS circuit that includes a structure in which a p-channel MOSFET or a p-channel spin MOSFET contained in the first circuit group is connected to an n-channel MOSFET or an n-channel spin MOSFET contained in the second circuit group with a shared drain terminal, and a first terminal that is formed at the shared drain terminal.

28. The circuit as claimed in claim 26, comprising

a CMOS circuit that is formed with a p-channel spin MOSFET contained in the first circuit group and an n-channel spin MOSFET contained in the second circuit group.

29. The circuit as claimed in any of claims 26 to 28, wherein the p-channel MOSFET or the p-channel spin MOSFET, and the n-channel MOSFET or the n-channel spin MOSFET of the CMOS circuit have a shared floating

gate forming a νMOS structure.

30. The circuit as claimed in claim 29, wherein the νMOS structure has two inputs (A and B) weighted with capacitances by capacitors.

31. The circuit as claimed in any of claims 26 to 30, wherein the circuit is an AND/OR reconfigurable logic circuit or a NAND/NOR reconfigurable logic circuit that includes an A-D converter having the first terminal as an input.

32. The circuit as claimed in any of claims 26 to 31, wherein the first and second circuit groups, or one of the first and second circuit groups comprises

a circuit that controls the potential of the first terminal by connecting the source or the drain of another spin MOSFET to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET, the level shift circuit turning on the another spin MOSFET only when a predetermined input is made.

33. The circuit as claimed in any of claims 26 to 32, wherein the second circuit group comprises

a circuit that controls the potential of the first terminal by connecting the drain of another spin MOSFET of n-channel type to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET of n-channel type, the another spin MOSFET of n-channel having the source grounded, the level shift circuit turning on the another spin MOSFET of n-channel type only when an input is A = B = "0".

34. The circuit as claimed in any of claims 26 to 33, wherein the circuit is an AND/OR/XNOR reconfigurable logic circuit or a NAND/NOR/XOR

reconfigurable logic circuit that includes an A-D converter having the first terminal as an input.

35. The circuit as claimed in any of claims 26 to 35, wherein the first circuit group comprises

a circuit that controls the potential of the first terminal by connecting the drain of the another spin MOSFET of p-channel type to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET of p-channel type, the another spin MOSFET of p-channel having the source connected to a supply voltage, the level shift circuit turning on the another spin MOSFET of p-channel type only when an input is A = B = "1".

36. The circuit as claimed in any of claims 26 to 35, wherein the circuit is an AND/OR/XOR reconfigurable logic circuit or a NAND/NOR/XNOR reconfigurable logic circuit that includes an A-D converter having the first terminal as an input.

37. The circuit as claimed in any of claims 26 to 36, wherein the circuit is a reconfigurable logic circuit that includes an inverter having the output of the A-D converter as an input, and can achieve all symmetric Boolean functions.

38. The circuit as claimed in claim 26 or 32, wherein the circuit is formed with a circuit group that is characterized by:

controlling the potential of the first terminal by connecting the drain of another spin MOSFET of n-channel type to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET of n-channel type, the another spin MOSFET of n-channel having the source grounded, the level shift circuit turning on the another spin MOSFET of n-channel

type only when an input is A = B = "1"; and

controlling the potential of the first terminal by connecting the drain of another spin MOSFET of p-channel type to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET of p-channel type, the another spin MOSFET of p-channel having the source connected to a supply voltage, the level shift circuit turning on the another spin MOSFET of p-channel type only when an input is A = B = "0".

39. The circuit as claimed in claim 38, wherein the circuit is an all symmetric Boolean function logic circuit that includes an A-D converter having the first terminal as an input.

40. The circuit as claimed in any of claims 32 to 39, wherein the level shift circuit is formed with an E/E, E/D, or CMOS inverter.

41. An A-D converter comprising

a CMOS inverter,

one of a p-channel MOSFET or an n-channel MOSFET of the CMOS inverter being a spin MOSFET, or a p-channel MOSFET and an n-channel MOSFET of the CMOS inverter being spin MOSFETs.

42. The A-D converter as claimed in claim 41, wherein a logic threshold value can be changed according to the magnetization state of the spin MOSFET.

43. A logic circuit comprising

an A-D converter that has a variable logic threshold value and is connected to an output stage of a circuit having an analog output, the logic circuit being capable of reconfiguring a logic function.

44. A circuit comprising

a transistor with variable transfer characteristics,

the circuit being capable of reconfiguring a function by moving an operating point through a change in the transfer characteristics of the transistor.

45. An integrated circuit comprising

the circuit as claimed in any of claims 1 to 44.